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Abstract
The existence of self-timed systems has been developed for years. Although this type of design methodology has already been proven low-power, highly-robust, easy to modularization, discrete and tiny EMI source, it avoids inductive problems such as global clock adoption. Also, since the design tools for the asynchronous system are not well-organized, most of designed engineers lack of knowledge in manipulation of the complex asynchronous design flows. In summary, this is why asynchronous circuit design is unable to dominate over the synchronous.
In addition, incompleteness of the high-level synthesis tool will lead to scheduling problem of the design flow, and engineer training program. Therefore, we propose a concise high-level synthesis tool which allows asynchronous designers to implement the HDL in the algorithmic-level-like behavioral description, and a way of verifying the translated language itself on the FPGA. We are capable of downloading HDL that contains extended burst-mode controller and the HDL generated by the traditional FPGA synthesis tool onto the development board for the test.
This paper uses channel-level HDL as the prototype of the asynchronous circuit development and incorporate the channel packages developed by Dr. Chris J. Myers of the University of Utah for the purpose of simulation and verification based on the back-end synthesizable tool for 4-phase bundled-data handshaking description. This tool allows circuit designers to realize the self-timed system in the familiar manner with known HDL programming by ignoring the complicated communication protocol and its corresponding circuit behavior.
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